IN THE ABSTRACT

At page 17, line 2, delete "An" and substitute --A--.

IN THE CLAIMS

1. (Once Amended) An integrated circuit comprising:

a conductor comprising conductive materials to form device interconnections, the conductor being formed from a damascene structure; and

a liner surrounding at least three surfaces of the conductor, the liner imparting a random grain orientation in the conductive material of the conductor to improve [reliability] electromagnetic lifetime of the conductor.

Please **ADD** claims 2-25 as follows:

--2. An integrated circuit of claim 1, wherein the liner comprises material has a random grain orientation.

3. An integrated circuit of claim 1, wherein the liner comprises material of amorphous character.

4. An integrated circuit of claim 1, wherein the liner comprises a material chosen from of the group consisting essentially of titanium nitride, tantalum, and tantalum nitride.

5. An integrated circuit of claim 4, wherein the liner comprises material has a random grain orientation or amorphous character.

6. An integrated circuit of claim 1, wherein the liner comprises a material chosen from of the group consisting essentially of carbon, graphite, noble metals, near noble metals, the rare earth metals which have a random grain orientation or an amorphous character.

7. An integrated circuit of claim 1, wherein the liner comprises a layer of titanium nitride, the layer being between about 10 Angstroms and about 1000 Angstroms thick.

8. An integrated circuit of claim 7, wherein the layer of titanium nitride is about 50 Angstroms thick.

9. An integrated circuit of claim 8, wherein the layer of titanium nitride is a layer of N_2/H_2 plasma treated titanium nitride.

10. An integrated circuit of claim 1, further comprising a subliner.

11. An integrated circuit of claim 10, wherein the subliner is a layer of titanium.

12. An integrated circuit of claim 11, wherein the layer of titanium for the subliner is between about 10 Angstroms and about 300 Angstroms thick.

13. An integrated circuit of claim 1, wherein the conductive materials comprise at least one material chosen from the group consisting essentially of aluminum, copper and tungsten.

14. An integrated circuit of claim 13, further comprising a subliner comprising titanium.

15. An integrated circuit of claim 14, wherein the conductor has a thickness of about 3700 Angstroms.

16. A DRAM integrated circuit, comprising

a device layer have device features for implementing DRAM functions;

an insulating layer formed over the device layer, the insulating layer having at least one opening patterned therein that is aligned with the device layer, the opening having a bottom and walls;

a liner layer formed over the wall and bottom of the opening; and

a conductive material that fills the opening to form a conductor,

wherein the liner layer lines the walls and bottom of the opening for the conductor.

17. A DRAM integrated circuit of claim 16, wherein the liner imparts a random grain orientation in the conductive material of the conductor to improve reliability of the conductor.

18. A DRAM integrated circuit of claim 16, wherein the liner imparts a random grain orientation in the conductive material of the conductor to improve electromagnetic lifetime of the conductor.

19. A DRAM integrated circuit of claim 16, wherein the liner comprises material has a random grain orientation or amorphous character.

20. A DRAM integrated circuit of claim 19, wherein the liner comprises a material chosen from of the group consisting essentially of titanium nitride, tantalum, and tantalum nitride.

21. A DRAM integrated circuit of claim 19, wherein the liner comprises a layer of titanium nitride, the layer being between about 10 Angstroms and about 1000 Angstroms thick.

22. A DRAM integrated circuit of claim 16, wherein the liner comprises a material chosen from of the group consisting essentially of carbon, graphite, noble metals, near noble metals, the rare earth metals which have a random grain orientation or an amorphous character.

23. A DRAM integrated circuit of claim 16, wherein said DRAM integrated circuit comprises a subliner formed between the liner and the conductive material that fills the opening.

24. A DRAM integrated circuit of claim 23, wherein the subliner is a layer of titanium.

25. A DRAM integrated circuit of claim 24, wherein the layer of titanium for the subliner is between about 10 Angstroms and about 300 Angstroms thick.

26. A DRAM integrated circuit of claim 16, wherein the opening is a damascene structure.

27. A DRAM integrated circuit of claim 16, wherein the opening is a trench.--

REMARKS

Claim 1 has been amended to further clarify the subject matter regarded as the invention, and new claims 2-27 have been added to the application. Claims 1-27 are